Circuits Final Project: Adaptive-Biasing Differential Amplifiers

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Introduction

In Lab 9, we learned about current-mirror differential amplifiers, where we observed a differential amplifier with a fixed slew rate. The circuit response is slower when a large differential input is applied since the fixed bias current of the differential input stage limits the total output current, causing a load capacitance to be charged linearly. An adaptive-biasing amplifier can temporarily increase its bias current when given a large differential input, allowing the output to quickly catch up to the input when the output is connected as feedback.

The goal of this report is to learn about adaptive-biasing amplifiers, implement one in simulation using LTSpice, and to share our findings.

Background

The differential feedback amplifier (Figure 1) is set up in a similar manner to the amplifier in Lab 9, but the bias current of the amplifier is made signal dependent by adding additional current sources made up of two current subtractors (Figure 2). In Lab 9, the total current in the circuit was equal to the bias current, defined by $I_b = I_{total} = I_1 + I_2$. In the adaptive biasing circuit, the total current is dependent on both I_b and the difference between the input currents. This can be expressed as:

$$I_{total} = I_1 + I_2 = I_b + max(0, I_2 - I_1) + max(0, I_1 - I_2) \tag{1}$$

When the circuit is connected to a capacitor and the step response is measured, the output voltage changes to reach the input voltage from the step. In a standard differential amplifier, during a large amplitude step the output voltage increases linearly with a slope given by the slew rate. This is because V_{out} depends on the voltage through the capacitor, which follows the equation $I = CdV/dt$. In this case, $I_{out} = I_b$, which is constant. Therefore, the output voltage increases by a constant value limited by the current in the circuit.

In the adaptive-biasing differential amplifier, I_{total} in the circuit increases temporarily when the input voltages are different, which means that I_{out} also increases. Since V_{out} is controlled by the capacitor, the voltage can change at a faster rate. Therefore, the adaptive biasing circuits have the advantage of increasing the current in the circuit so that V_{out} responds faster to large changes in the input voltages. The rate of increase in V_{out} in the adaptive biasing circuit is much faster than the slew rate differential amplifiers without that.

Schematics

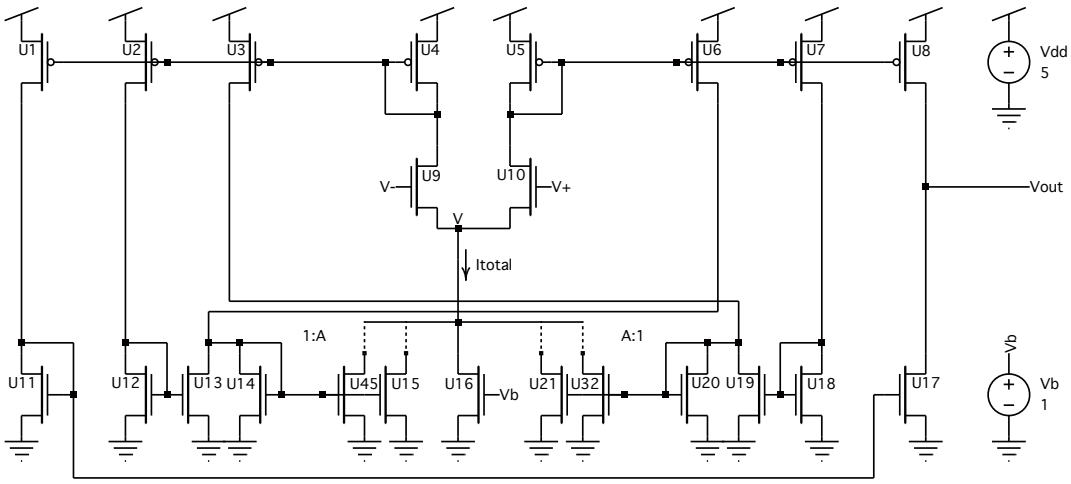

Figure 1: The schematic for an adaptive-biasing amplifier. The additional current source is realized by two subtractors (see Figure 2).

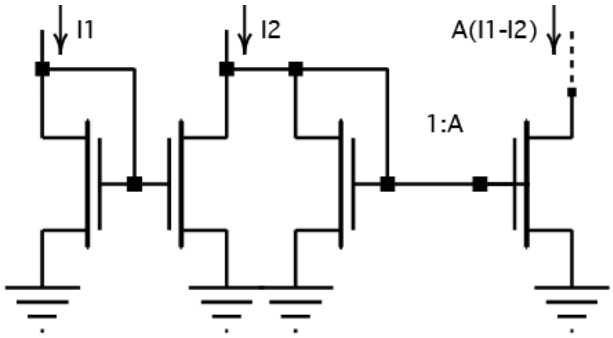

Figure 2: The schematic for the current subtractor realizing $A(I_2 - I_1)$. The current feedback factor (A) depends on the width of the transistor in the current mirror. Adding more transistors in parallel also has the same effect as using a transistor of a different size.

Results

Voltage Transfer Characteristics

The behavior of this adaptive-biasing amplifier (Figure 3) is very similar to the one in Lab 9, although it does not rail as well when V_+ and V_- are very different. This is because the adaptive-biasing increases the total current through the diff amp pair, which causes the current mirror transistors to be in strong inversion. Since the output stage current mirror transistors are in strong inversion, their V_{DSsat} increases, causing there to be a noticeable V_{DS} voltage difference from the rails in V_{out}. This does not affect the performance of the amplifier during normal use, because we care about the output voltage when the amplifier is in the high-gain region.

The differential-mode voltage gain was calculated from Figure 4 as $A_{dm} = 188.452$. The differential-mode voltage gain does not change for different values of A, as expected. Furthermore, the value of A_{dm} found through simulation is reasonably close to the value found in Lab 9.

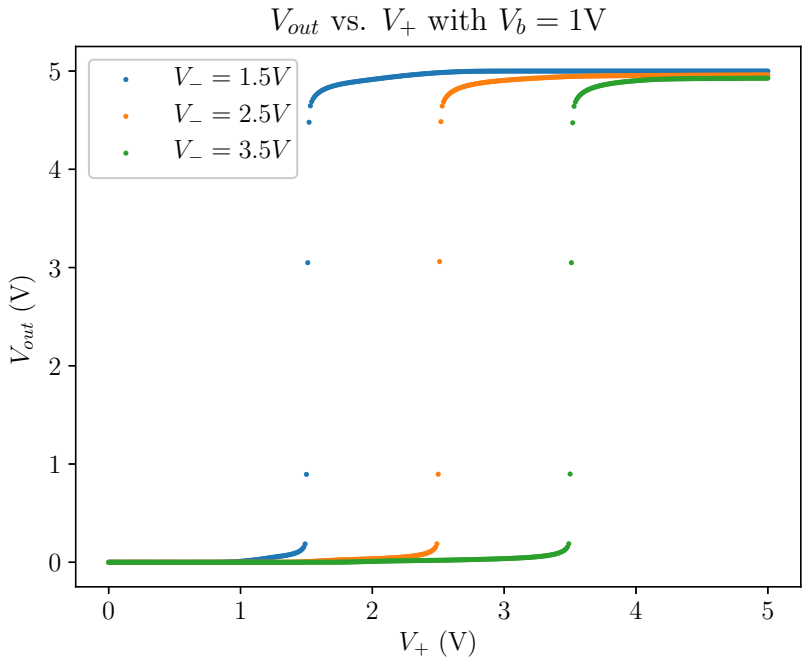

Figure 3: V_{out} as a function of V_+ for three values of V_-, with $V_b = 1$V and $A = 1$.

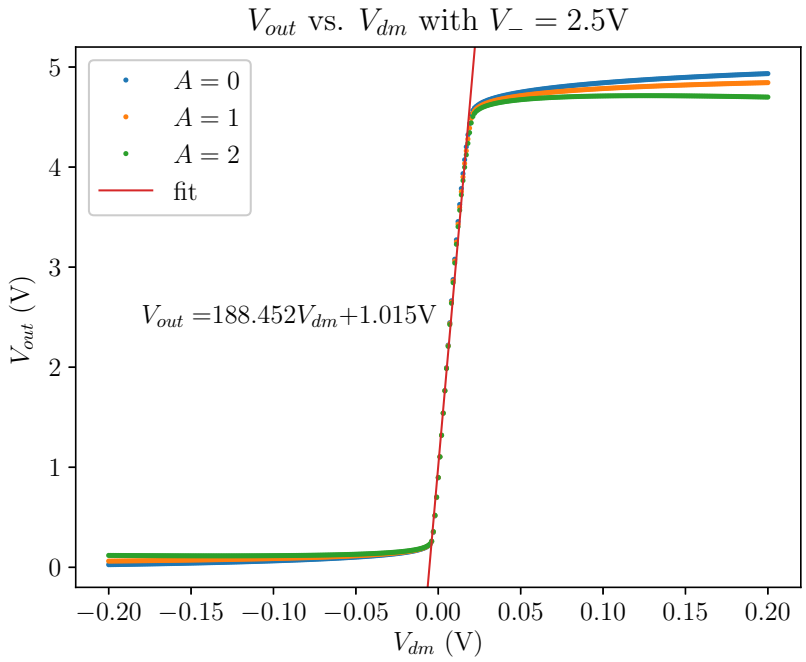

Figure 4: V_{out} as a function of V_{dm} for various values of A, where the slope of the fit equals the incremental differential-mode voltage gain of the circuit.

Current Voltage Characteristics

Keeping V_{out} and V_2 fixed at 2.5V, we swept V_1 around V_2 from 2V to 3V and measured the current flowing out of the amplifier as V_{dm} goes from negative to positive values.

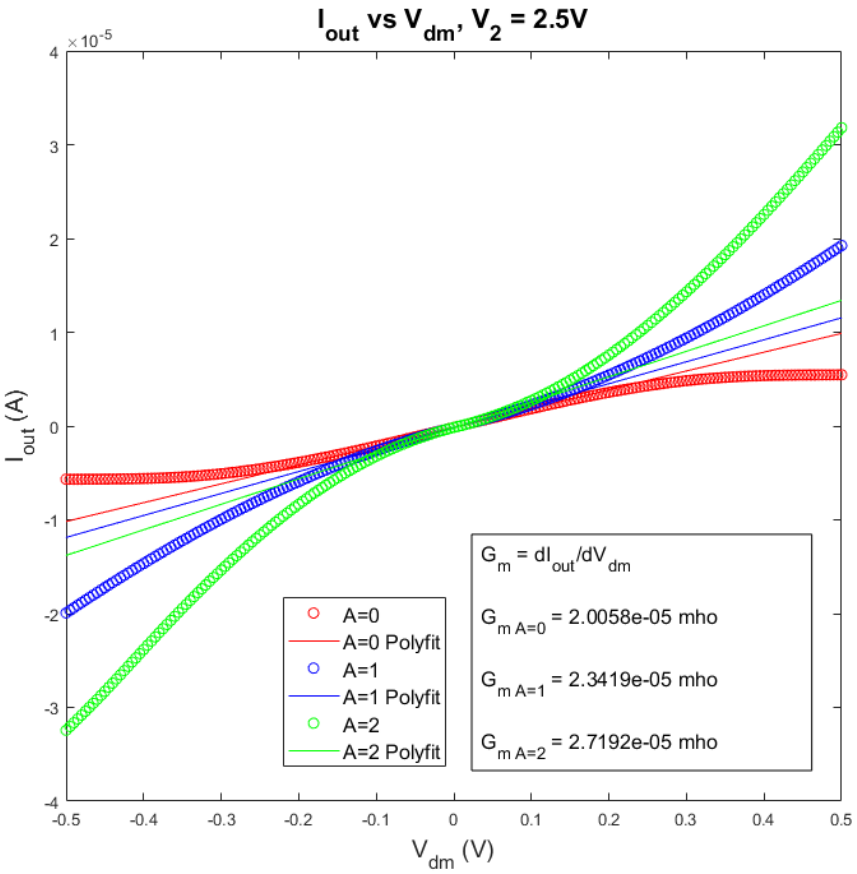

Figure 5: I_{out} as a function of V_{dm} for various values of A, along with their fit lines.

Using the Polyfit function, we fit straight lines to the curve around where $V_{dm} = 0$. From there, we extracted the incremental tranconductance gain, G_m, which was found by taking the slope of the fit line since $G_m = \delta I_{out}/\delta V_{dm}$. Figure 5 shows that as A increases, G_m also increases as the output current is increasing. When A = 0, the current tapers on both ends as it nears the bias current. However, when A is greater than 0, the output current is not limited by the bias current and does not flatten at either end.

Large Amplitude Step Response

We connected the adaptive-biasing differential amplifier circuit as a unity-gain follower, by connecting the inverting input to the output, which was then connected to ground through a 10pF capacitor. We simulated the large amplitude step response of this circuit for different values of the current feedback factor.

The setup with a current feedback of A=0 behaves as if there is no subtractor in the circuit, so we expect the step response to be the same as a standard differential amplifier, such as the circuit in Lab 9. In Figure 6 on the following page, the step response for a circuit with A = 0 rises linearly where the slope is defined as the slew rate. We expect the slew rate to be I_b/C, where our $I_b = 5.4\mu A$ and C = 10pF. Therefore, we expect the slew rate to be 5.4×10^5 V/s. Based of a best fit line of the data, the slope of the line is 5.5 V/s, which is close to the predicted value.

In comparison, the step response was also measured for the differential amplifier with current-feedback values of a=1 and a=2. Because these subtractor allows the current through the circuit to increase based on the difference between the two input currents, it allows the output voltage to follow changes in the input voltage more quickly. Since the current is no longer constant, the rate of voltage increase is no longer linear. Figure 7 on the next page shows the same three circuits with an input step of a shorter period.

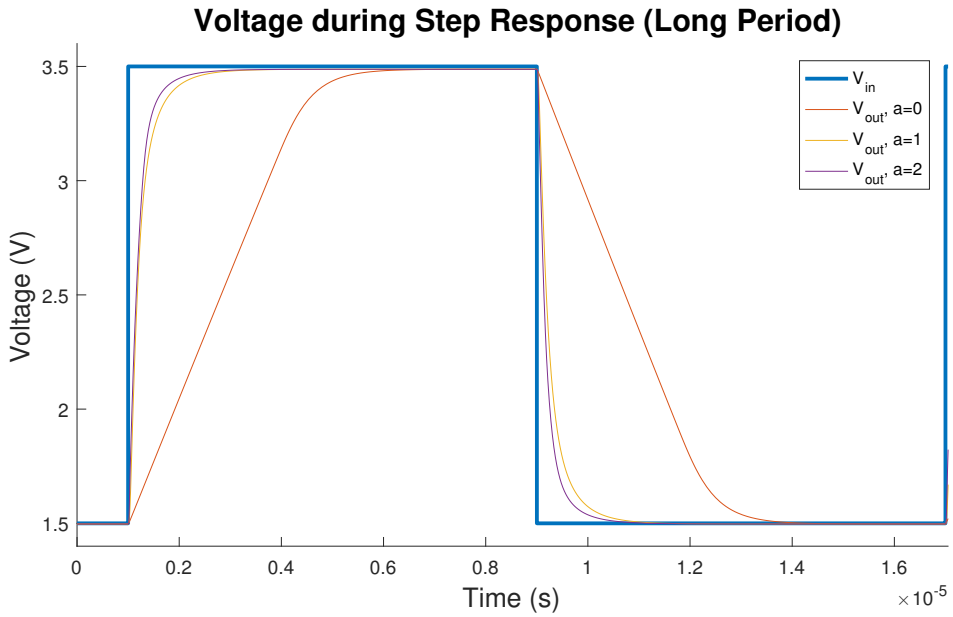

Figure 6: Output voltage over time for various values of A, for a large amplitude step response.

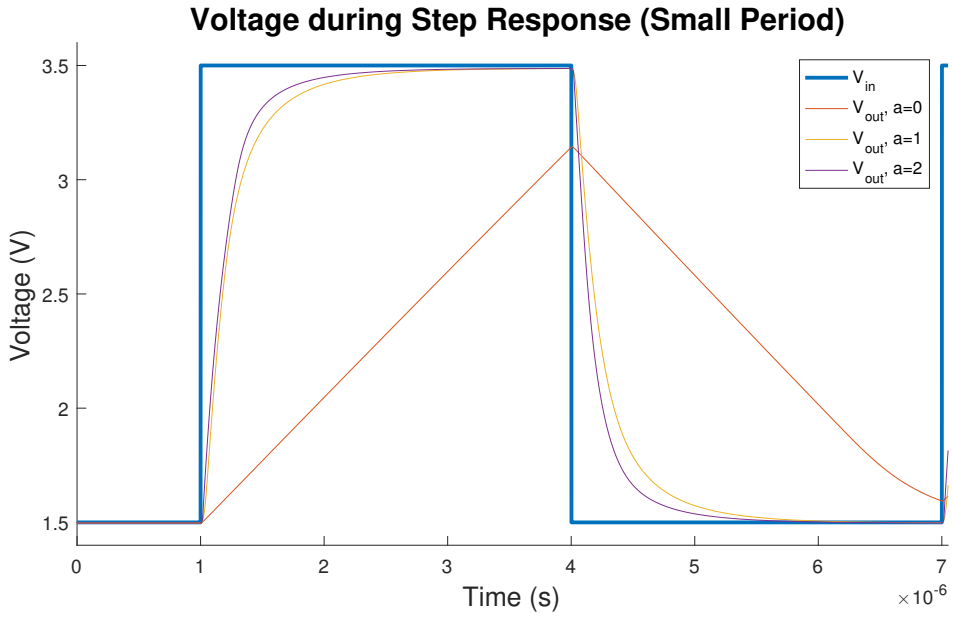

Figure 7: Output voltage during a step response with the same amplitude as Figure 6. This step has a shorter period to show the distinction between the response for different values of A.

In the circuits with a subtractor, the V_{out} value rises much more quickly in response to a large amplitude step response, especially as compared to the standard differential amplifier circuit. Between the two circuits with different values for current feedback, the one with a feedback of A=2 rose slightly more quickly than the circuit with A=1, but this is not a significant difference in relationship to the original differential amplifier circuit. Table 1 has a comparison of the time it takes for each circuit's output to reach the input voltage value.

The reason the adaptive biasing differential amplifier responds more quickly to the step change is because there is more total current flowing through the circuit (denoted by I_{out} in the circuit diagram). This current

Table 1: Comparison of time it takes for the output voltage to reach the maximum value, for different values of current feedback.

Current-Feedback Value	Time to Reach Max Voltage (s)
A = 0	6.2×10^{-6}
A = 1	3.3×10^{-6}
A = 2	2.8×10^{-6}

is proportional to the current flowing out of the circuit and through the capacitor. Since current through the capacitor is described by $I = CdV/dt$, when there is more current through the capacitor, it allows the voltage to change more rapidly. Therefore, by allowing more current to flow through the circuit, it increases the rate at which V_{out} can follow V_{in}.

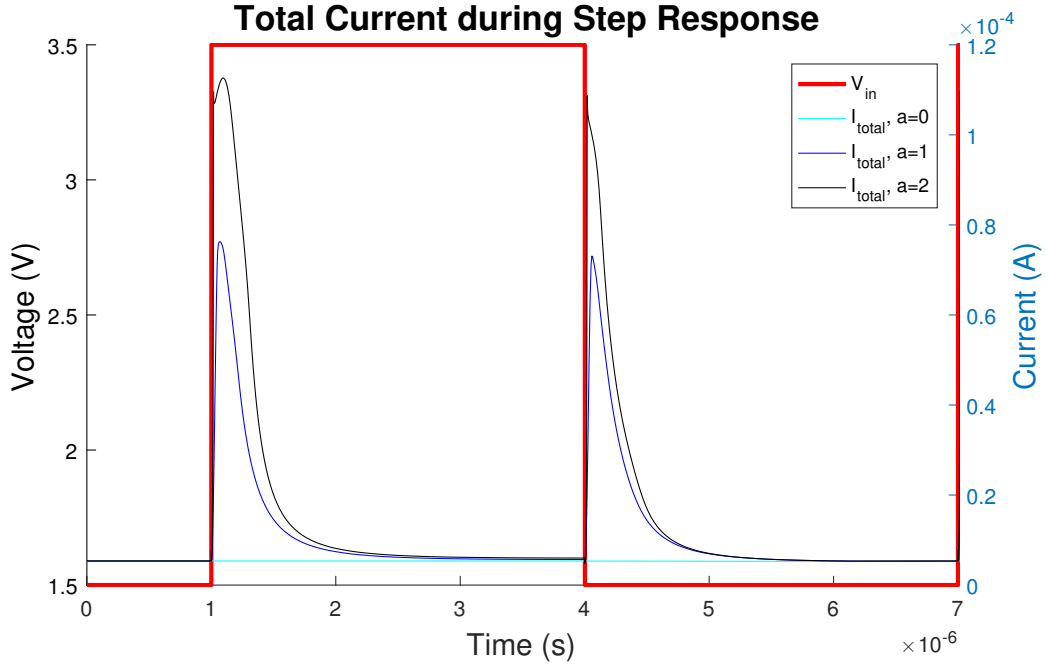

Figure 8: Current in the circuit over time, during a step response. The input voltage is also graphed for reference.

This behavior is reflected in Figure 8, where the total current through the circuit is plotted for different values of A as a function of time. The V_{in} square wave is also plotted for reference. At the instant that V_{in} has a step up, V_{dm} in the circuit increases so the difference $I_2 - I_1$ also increases. Because of the subtractors present in the adaptive biasing circuit, this increases the total current in the circuit right after V_{in} steps up or down. After a long time, V_{out} is adjusted to match V_{in}, so there is no current difference and the total current in the circuit drops down the baseline level. For comparison, the differential amplifier with no adaptive biasing is also shown, and the current through that circuit is always constant.

Discussion

Unlike the Lab 9 diff amp, this one with adaptive bias did not defy us,
Vout responds to large amplitude steps not just depending on the bias.
The current through the capacitor increases by the difference of the input,
Because the subtractor adds current to increase the total throughput.
Increasing the current feedback factor changes the voltage at a faster rate,
At a cost of two more transistors per unit increase, so building this circuit isn't great.
We used LTSpice to measure DC sweeps and step responses in simulation,
So we could use the graphs to analyze properties of this creation.

Acknowledgments

Thanks Brad!

References

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2. Adaptive biased operational amplifier with improved Slew-Rate: Overview with graphs of the expected voltage characteristics and transient circuit responses. (http://ieeexplore.ieee.org/document/6317391/?reload=true)
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